REMARKS

Claims 21-50 were pending in the application. Claims 22-27 were withdrawn from consideration. Claim 21 has been amended. Claims 33 and 34 have been cancelled. Claims 21, 28-32 and 35-50 remain pending and under consideration in the present application.

Objection to the Claims:

Applicant has amended claim 21 in accordance with the Examiner's suggestion. Removal of the objection is respectfully requested.

35 U.S.C. § 102 and § 103 Rejections:

Claims 21, 28-32, 37-46, and 49-50 were rejected under 35 U.S.C. §103(a) as being unpatentable over Weiblen, U.S. Patent 6,528,868 in view of Hanzawa, U.S. Patent 6,538,866, Lee, U.S. Patent 6,852,567, and Applicant's Admitted Prior Art (APAA), Fig. 2, Page 3. Applicant respectfully traverses this rejection.

The cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims. The teachings of Weiblan were presented in the previous office action response. Hanzawa teaches a circuit for protecting a load from an overvoltage can be integrated together with the load on the same chip by an MOS transistor manufacture process. This overvoltage protecting circuit is composed of a surge protection circuit, an overvoltage detecting circuit and a switching circuit. The surge protection circuit including two MOS transistors operates so that a surge voltage applied to a power supply receiving terminal is clamped by virtue of the source-drain breakdown voltage of the two MOS transistors, thereby absorbing the surge energy. The overvoltage detecting circuit including two MOS transistors operates so that a DC voltage supplied from the surge protection circuit is monitored with the source-drain voltage of the two MOS transistors taken as a reference voltage, thereby detecting an overvoltage. An overvoltage detection output brings an MOS transistor of the switching circuit into a turned-off condition to protect the load.

Lee teaches a method of assembling a semiconductor device package including first attaching a semiconductor device to a die-pad area of a leadframe. Electrical connections are then between electrical contact areas on the semiconductor device and electrical connection areas on the leadframe to form a device/leadframe assembly. An adhesion enhancing coating is then deposited on the exposed surface of the device frame/leadframe assembly before encapsulating the coated device leadframe assembly in an electrically insulating material.

In contrast, Applicant's independent claim 21 recites, in pertinent part:

"A semiconductor device, comprising:

a first die attach paddle made of an electrically conductive material, wherein the first die attach paddle is electrically coupled exclusively to analog circuitry;

a second die attach paddle made of an electrically conductive material, wherein the second die paddle is electrically coupled exclusively to digital circuitry; and ...

wherein the first and second die attach paddles are connected to provide ground contacts for analog and digital signals, respectively, wherein the semiconductor device comprises an analog ground associated with the analog circuitry and a digital ground associated with the digital circuitry, wherein the analog and digital grounds are separate from each other" (Emphasis added).

None of the cited references, whether taken singly or in combination, teach or suggest the combination of features recited in claim 21. As noted in the previous office action response, Weiblen does not provide any teaching as to whether processor chip 200 and sensor chip 201 are analog, digital, or mixed signal integrated circuits. The Examiner contends that Weiblen discloses that sensor chip 201 is analog circuitry and that processor chip 200 is digital circuitry, but as a basis of support, appears to cite Hanzawa at Figs. 8-9 and col. 8, lines 7-45 for [an] evidence. However, in col. 8, lines 10-12,

signal processing chip 21 of Hanzawa is described as including an analog circuit 22, a logic circuit 23, and a memory circuit 24. Similarly, in col. 8, lines 38-40, sensor chip 31 of Hanzawa is also described as including an analog circuit 22, a logic circuit 23, and a memory circuit 24. Thus, the combination of Weiblan and Hanzawa proposed by the Examiner does not teach or suggest a first die attach paddle is electrically coupled **exclusively** to analog circuitry and a second die attach paddle made of an electrically conductive material, wherein a second die paddle is electrically coupled **exclusively** to digital circuitry as recited in claim 21. Furthermore, neither Lee nor APAA provide any teaching or suggestion, that when combined with Weiblan and/or Hanzawa would result in such a combination of features.

Furthermore, none of the cited references, whether taken singly or in combination, teach or suggest a semiconductor device comprising "an analog ground associated with the analog circuitry and a digital ground associated with the digital circuitry, wherein the analog and digital grounds are separate from each other." Furthermore, none of the references provide any teaching, suggestion, or motivation for providing separate analog and digital grounds that are coupled to first and second die attach paddles are exposed on the bottom surface of a semiconductor device package.

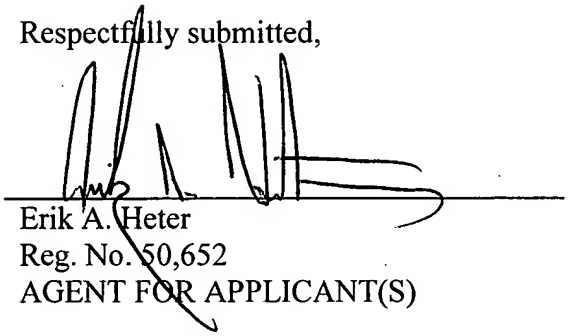
For at least these reasons, Applicant submits that a case of obviousness has not been established. Accordingly, removal of the 35 U.S.C. §103(a) rejection is respectfully requested.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-79302/EAH.

Respectfully submitted,



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